REMARKS

The Examiner has objected to the Drawings for the reasons noted on the Notice of Draftsperson's Patent Drawing Review, Form PTO-948. Applicants will provide Formal Drawings overcoming these objections after allowance of the claims.

Rejections Under 35 U.S.C. §102

Claims 1-5 and 14-19 have been rejected under 35 U.S.C. 102(e), as being anticipated by U.S. Patent No. 5,859,791, issued Jan. 12, 1999 to Schultz et al. (hereinafter "Schultz"). The Examiner states that:

> Figure 9 of Kim [sic] is directed to a content addressable memory cell comprising: a static random access memory cell, SRAM, (latch of Fig. 9) for storing a data value; a first set of one or more bit lines (bl and bln) wherein the data value is written to and read from the SRAM cell; a second set of bit lines (k and kn) coupled to receive a comparison data value.

Applicant assumes that Examiner intended to refer to Schultz (rather than "Kim"), as prior reference had been made to Schultz, and the subsequent figure and specification references are consistent with Schultz. Applicant respectfully traverses this rejection.

Claims 1-5

Claim 1 recites:

> A content addressable memory (CAM) cell comprising:
> a static random access memory (SRAM) cell that operates in response to a VCC supply voltage … ;
> a first set of one or more bit lines coupled to the SRAM cell … having a signal swing equal to the VCC supply voltage; and

a second set of bit lines coupled to receive a comparison data value, the second set of bit lines having a signal swing less than the VCC supply voltage. (Emphasis added.)

The present invention teaches the use of a compare operation that operates within a voltage range that is less than the voltage range of the associated read/write operations. (Specification, page 5, lines 25-32.) "By lowering the supply voltage required to perform a compare operation, the power of operating the CAM is advantageously reduced." (Specification, page 5, lines 30-32.)

Just as in the present invention, one of the specified goals of Schultz is "achieving low power dissipation." (Schultz, col. 2, line.) (Emphasis added.) Towards this end, Schultz describes in Fig. 9 a "memory core cell" having separate "compare bit lines k/kn … separate … from the normal bit line pair bl/bln, … [which] decreases the capacitive load on each, hence decreasing power dissipation and increasing speed." (Schultz, col. 7, lines 22-26.) However, Schultz fails to teach or suggest that the separate compare lines operate with "a signal swing less than the VCC supply voltage", as recited in Claim 1. For this reason, Claim 1 is allowable over Schultz. Claims 2-5 depend from Claim 1 and are therefore allowable over Schultz for at least the same reasons as Claim 1.

Claims 14-19

Claims 14-19, which also depend from Claim 1, are allowable over Schultz for at least the same reasons as Claim 1.

Claim 16 recites a bit line control circuit for "connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply

line having a voltage less than the VCC supply voltage." (Emphasis added.) This reduced voltage advantageously allows the masking voltage applied to the compare lines to be consistent with a "signal swing less than the Vcc supply voltage", as recited in Claim 1. As described previously, Schultz does not teach or suggest the use of such a reduced-voltage signal swing. Consequently, Schultz would have no reason to provide a masking voltage "less than the Vcc supply voltage" as recited in Claim 16. Claim 16 is allowable over Schultz for this additional reason.

Claim 17 recites a bit line control circuit for "selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, … the voltage supply line having a voltage less than the Vcc supply voltage." (Emphasis added.) This selective coupling operation provides means for the "signal swing less than the Vcc supply voltage" recited in Claim 1 to be applied to the second set of bit lines. As described previously, Schultz does not teach or suggest the use of such a reduced voltage signal swing. Thus Schultz would have no reason to selectively couple compare lines to ground and "a voltage less than the Vcc supply voltage", as recited in Claim 17. Claim 17 therefore is allowable over Schultz for this additional reason.

Claim 18 depends from Claim 17 and further recites that "the voltage supply line has a voltage of two times a transistor threshold voltage." (Emphasis added.) As described previously, Schultz does not teach or suggest even a reduced compare line voltage, and certainly does not describe a compare line voltage of "two times a transistor threshold voltage." Claim 18 therefore is allowable over Schultz for this additional reason.

Claim 19 recites a "bit line control circuit … powered by a supply voltage less than the Vcc supply voltage." (Emphasis added.) The lowered supply voltage allows the bit line control circuit to "[operate] in response to a supply voltage Vcc1, which is much less than the Vcc supply voltage … [so] the power requirements of CAM cell 100 are much less than a conventional 9-T CAM cell." (Specification, page 9, lines 20-27.) Just as Schultz does not teach or suggest a lowered-voltage compare operation, neither does Schultz teach or suggest a circuit for providing those reduced compare voltages. Claim 19 is therefore allowable over Schultz for this additional reason.

Claim 20

Claim 20 has been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,351,208, issued Sep. 27, 1994 to Jiang (hereinafter "Jiang"). Applicant respectfully traverses this rejection.

Claim 20 recites a CAM cell "having a match line … having a signal swing equal to one transistor threshold voltage." (Emphasis added.) As described previously, a reduced operating voltage for match operations advantageously decreases power consumption in a CAM cell. The Examiner has rejected Claim 20 by stating that Fig. 2 of Jiang discloses a match line (214) "having a signal swing equal to one transistor threshold voltage (0V-Vt of 75)." The Examiner seems to indicate that match line 214 of Jiang carries a signal controlled by the node between transistors 210 and 211, and that signal varies between 0V and Vt.

However, contrary to the Examiner's rejection, Jiang does not teach or suggest that the signal swing on match line 214 is equal to "one transistor threshold voltage" as recited in

Claim 20. Applicant notes the Examiner's contention that such an operating condition is described by Jiang, but cannot relate the Examiner's reference ("0V-Vt of 75) to any portion of Jiang. Jiang simply states that "match line 214 [is] precharged for the comparison operation." (Jiang, col. 2, lines 55-56.) Jiang does not describe any special precharging circuit or source. Nor does Jiang indicate that match line 214 is precharged to a special voltage. This lack of detail strongly implies that the precharging is to supply voltage Vcc, and Jiang certainly does not describe a precharging voltage that would enable match line 214 to have a "signal swing equal to one transistor threshold voltage" as recited in Claim 20. Claim 20 is therefore allowable over Jiang.

Claims 21-32

The Examiner has rejected Claims 21-32 under 35 U.S.C. 103 for the same reasons as Claims 1-5 and 14-19, since they "encompass the same scope of invention … except they [are] draft[ed] in method format instead of apparatus format." However, Claims 1-5 and 14-19 are allowable for the reasons stated above. Therefore, Claims 21-32 are allowable for similar reasons.

Rejections Under 35 U.S.C. §103

Claims 6 and 8-13

Claims 6 and 8-13 have been rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over Schultz. The Examiner states that:

> Schultz discloses all of the subject matter except for … a diode element … [h]owever, Figure 9 of Schultz shows a transistor 723 connected to the first node … an equivalent structure known in the art. Therefore, because these two diode element and transistor were art-

> recognized elements at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the transistor for the diode element whose on or off state controlled by a state of the first node. (Emphasis added.)

Applicant respectfully traverses this rejection.

Transistor 723 of Schultz does not function as a diode, but rather, as a switch. Transistor 723 "forms a part of the match line chain … with its source and drain connected … to similar FET in neighboring cells." (Jiang, col. 7, lines 17-20.) If all transistors in the match line chain are on, then a match condition is indicated. Otherwise, a no-match condition is indicated. A diode will not perform this switching function and is therefore not "an equivalent structure". Claim 6, which recites "a diode element coupled to the first node", is therefore allowable over Schultz under 35 U.S.C. 103(a). Claims 8-13 depend from Claim 6, and are therefore allowable over Schultz for at least the same reason as Claim 6.

Claim 11 recites a CAM cell "wherein the match line has a signal swing equal to a transistor threshold voltage." Schultz, on the other hand, teaches a match line comprising a chain of transistors (see Fig. 5A of Schultz). Such a match line has no definite signal swing, since the line is floating unless all transistors in the chain are turned on. Therefore, Schultz does not teach or suggest a "signal swing equal to a transistor threshold value" as recited in Claim 11. (Emphasis added.) Claim 11 is allowable over Schultz for this additional reason.

Claim 12 recites "a sensor circuit pre-charging the match line to a voltage less than the Vcc supply voltage." By pre-charging the match line to an appropriate reduced voltage level, the low power match operation can be properly

performed. The chained match line taught by Schultz teaches away from pre-charging, since all the transistors in the chain are turned off (non-conducting) at the start of a match operation. Claim 12 is therefore allowable over Schultz for this additional reason.

Claim 13, which depends from Claim 12, recites a sensor circuit comprising "a logic gate for providing an output signal that indicates whether a match or no-match condition exists, the output signal having a signal swing equal to the Vcc supply voltage." (Emphasis added.) The sensor circuit, which is "coupled to the match line" as recited in Claim 12, therefore detects and converts the reduced-voltage match line signal into a full-voltage output signal. Schultz, as described previously, does not teach a reduced match line signal swing, and so does not teach or suggest any sensor circuit for detecting and converting such a signal. Claim 13 is allowable over Schultz for this additional reason.

Claim 7

The Examiner has indicated that Claim 7 would be allowable if rewritten as an independent claim, incorporating all the limitations of any intervening claims. However, Applicant has chosen not to amend Claim 7 at this time. Applicant contends that Claim 6 is allowable in view of the foregoing remarks. Claim 7 therefore is allowable for at least the same reasons as Claim 6.

CONCLUSION

Claims 1-32 are pending in the present Application. Reconsideration and allowance of Claims 1-32 is respectfully requested. If there are any questions, please telephone the undersigned at (408) 451-5903 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: BOX NON-FEE AMENDMENT, Assistant Commissioner for Patents, Washington, D.C., 20231, on January 24, 2000.

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